ISSN(O): 2320-5407 | ISSN(P): 3107-4928

International Journal of Advanced Research

Publisher's Name: Jana Publication and Research LLP

www.journalijar.com

REVIEWER'S REPORT

Manuscript No.: **IJAR-58800**

Title: Four bit Counter Using Verilog.

Recommendation:

Accept as it is .....

Accept after minor revision.....

Accept after major revision √.....

Do not accept (*Reasons below*) .....

Rating	Excel.	Good	Fair	Poor
Originality			√	
Techn. Quality		√		
Clarity		√		
Significance			√	

Reviewer's ID: JPR- Dr PRITI GUPTA

Detailed Reviewer's Report

1. There are several grammatical and formatting issues throughout the manuscript.
2. "Verilog" and "VHDL" are sometimes discussed interchangeably. The manuscript should maintain clear distinction between them.
3. The phrase **"In the context of VHDL"** in the device-utilization section is inappropriate because the proposed design is implemented using Verilog.
4. Figures should have consistent numbering and captions.
5. The technology schematic on page 5 is difficult to interpret at the presented scale and should be provided in higher resolution.
6. The simulation waveform figures should have larger labels and clearer captions.
7. The references should be formatted according to the journal's prescribed reference style.
8. The conclusion is too brief and should summarize the principal quantitative results and limitations. The current conclusion mainly states that the counter was implemented, simulated, and synthesized.